IBM 360/370/3090/390 Model Numbers

- 360/20 - the smallest S/360 was not really a compatible member of the family. It had only half the registers, and the instruction set was a subset that was not binary-compatible. I seem to remember that it had the capacitive punched-card microprogram storage, so that a 1401 emulation instruction set could be field installed.
- 360/25 - what the model 20 **should** have been. A relative latecomer to the family. Also had writable control store.
- 360/30 - the low-end workhorse, running DOS (or TOS - Tape Operating System).
- 360/40 - the midrange workhorse. This may have been the most popular machine of the series.
- 360/44 - the oddest model. It could be described as a 40 with a hardware floating point processor and faster memory. Had a variable precision floating point unit that could operate on *4, *5, *6, *7, and *8 byte operands. A rotary switch on the front panel could select between 2 different floating point formats. It had only 1/2 word and 1 word instructions and could therefore use a one word memory width without any speed penalty. Due to the odd instruction set, it had its own operating system, PS/44.
- 360/50
- 360/65
- 360/67 - the precursor to the S/370 family: The only 360 model with virtual memory support. Was also available in a dual-processor version.
- 360/75 - the fastest of the original 360s. Had the entire S/360 instruction set implemented in hardwired logic (all the others had microcode). Ran at one MIPS.
- 360/85 - 1969 - the first production machine with cache memory. Other 360 novelties in this model were extended-precision (16-byte) floating point, relaxation of some instruction operand alignment requirements, and an optional I/O channel which allowed multiple disk channel programs to run (sort of) concurrently. These later became standard in 370's. Writable control store?
- 360/91 - the first pipelined processor. Fully hardwired. Most of the decimal instructions were missing (emulated in software). Because it had multiple instruction execution units, it had "imprecise interrupts". When an interrupt or an exception occurred, the program counter might not point to the failing instruction if the multiple execution units were all active at the same time. For this reason, it was advisable to put NOPs around instructions that might lead to exceptions. Not many of these were built, and they may all have had slightly different tweaks as each of them was successively hand built by the same engineering team.
- 360/95 was a 91 equipped with a higher-performance thin-film memory instead of core. Only a couple were built.
- 360/195 was a faster successor to the 91, again fully-hardwired. It came in both 360 and (later) 370 versions. The 370 version had the new 370 instructions plus the 370 TOD clock and control registers, but not virtual-memory hardware. Also had imprecise interrupts.
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- 370/165 - 25 ns cycle time. Fastest general purpuse mainframe in early 1970s. 2.1 average cycles per instruction.
- 370/168 - same as 360/165 with dynamic address translation (virtual memory) added. Also larger cache pushed performance to 1.6 cycles per instruction. Density: 4 circuits per chip. 168-3 was 3.5 Mips
- 3033 - last top-of-the-line before the TCM (Thermal Conduction Module) packaging. Cycle time may have been 51 ns. Density about 40 circuits per chip, allowing 4.5-5 Mips. 303x machines were 370 architecture, with 24 bit logical address space (but 26 bit = 64MB max physical memory).
- 4361 - small cpu, used as service (maintenance) processor for 3090
- 4381 - a larger mini

- 3081 - First TCM based machine. Cycle time around 30 ns (+-3). 308x machines were XA architecture. 3081 was a dual-processor; the first dual that could not be split into two separate systems.
  - 3083 - a single-processor version of the 3081, built for the ACP/TCF (airline reservation systems) customer community, since ACP did not support multi-processing. 3083 was slightly less expensive than 3081, but gained a 15% performance increase over running a single processor on the 3081 (because it omitted the cache synchronization logic).
  - 3084 - a twin-3081: i.e. a 4-way system that could be split and run as two two-way machines.
- 3090 series: 12.5 ns cycle time

From Dave Glass (glass2@glass2.lexington.ibm.com)

From a copy of IBM System/370 System Summary: Processors (GS22-7001-18) (January 1987):

[1]=The "Processor basic machine cycle time" (nanoseconds)
[2]=Storage access width (number of bytes fetched per access)
[3]=Storage cycle time, (nanoseconds)
[4]=Storage Interleaving

	3115-0 3115-2	3125-0 3125-2	3135	3135-3	3138	3145	3145-3	3148	3158 3158-3	3168 3168-3
[1]	480	480	275- 1485	275- 1485	275- 1485	202.5- 315	180- 270	180- 270	115	80
[2]	2	2	2/4	2/4	2/4	8	8	8	16	8
[3]	480	480, 320	770- 935 rd 935 wr	770- 935 rd 935 wr	715- 880 rd 935 wr	540 rd 607.5 wr	405 rd 540 wr	405 rd 540 wr	1035 rd 690- 920 wr	320 A
[4]	-	-	-	-	-	-	-	-	-	4-way

A=The storage cycle times given for the 3168 do not reflect the time reductions that result from storage interleaving or, additionally, for 3168 and 3168-3 tie reductions resulting from the use of the high-speed buffer.

	3031	3032	3033	3033 MG-N	3033 MG-S	3081	3083	3084	3090
[1]	115	80	57	57	57	24, 24.5, 26	24, 24.5 26	24, 24.5 26	-
[2]	8	8	8	8	8	8	8	8	-
[3]	345	320	342	342	342	312	312	312	-
[4]	4-way	4-way	4-way	4-way	4-way	2-way	2-way	2-way	-

As for the IBM S/360 machines, here's a summary from a table in appendix D of the book 'Programming the IBM 360' by Clarence B. Germain (1967):

360 MODELS

#	Core Size	25	30	40	50	65	75	85	91-95	44	67	20
B	4K	X										X
C	8K	X		X								X
D	16K	X		X		X						X
E	32K	X		X		X				X		
F	64K		X		X		X			X		
G	128K		X		X		X			X		
H	256K		X		X		X		X		X	
I	512K		X		X		X		X		X	

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J     1024K.................X...X...X...X.....X........X......
K     2048K.............................X.....X........X......
L     4096K.............................X.....X..............
2361  1024K..................X...X...X.........................
2361  2048K..................X...X...X.........................
CD      24K.....................................................
DE      48K.....................................................

Cycle time(uS)  .9  1.5 2.5 2.0 .75 .75 1.04 .75-.125 1.0 .75 3.6
  per _ bytes    2  1   2   4   8   8   16   8         4   8   1
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This agrees with the information contained in my copy of 'IBM Field Engineering Education Student Self-Study Course' SR23-3062-7 (November 1973).

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$Log: model360.htm,v $
Revision 1.3  2003/01/03 16:27:56  lars
*** empty log message ***

Revision 1.2  2001/10/26 13:28:02  lars
Replaced CMC -> Beagle-Ears

Revision 1.1  2001/01/04 05:15:13  lars
Added file of S/360 Models
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